

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Shinji ITAMI

Appln. No.: 09/980,098

Group Art Unit: Not Yet Assigned

Confirmation No.: 1120

Examiner: Not Yet Assigned

Filed: November 29, 2001

For: DATA TRANSMISSION SYSTEM


SUBMISSION OF FORMAL DRAWINGS

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith please find nineteen (19) sheets of formal drawings. The Examiner is respectfully requested to acknowledge receipt of these formal drawings.

Respectfully submitted,

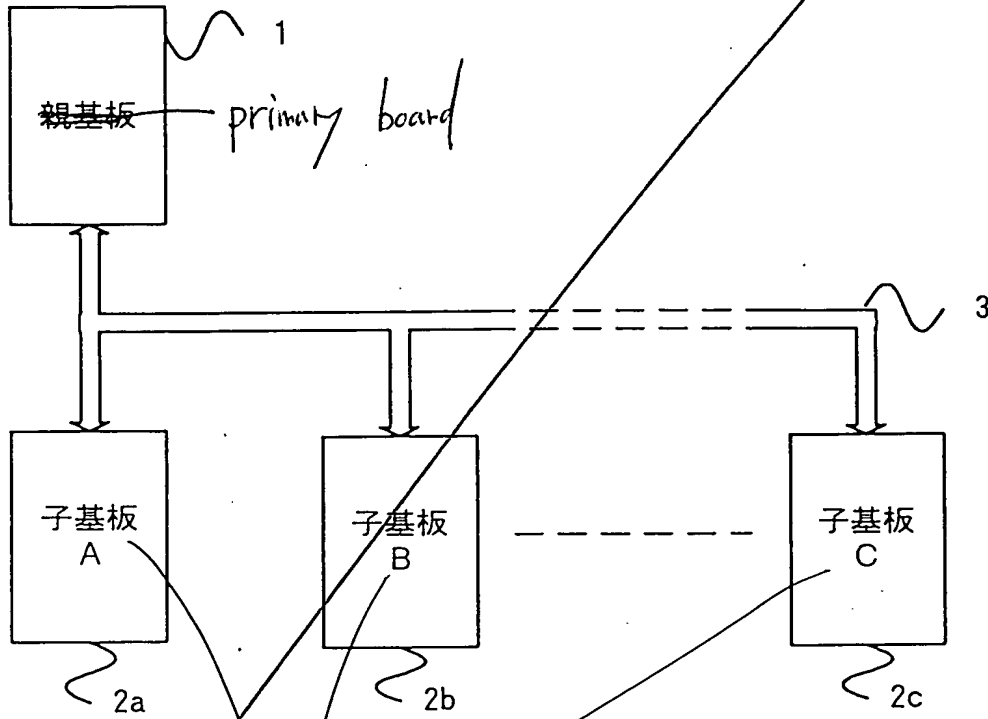


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Date: March 15, 2002

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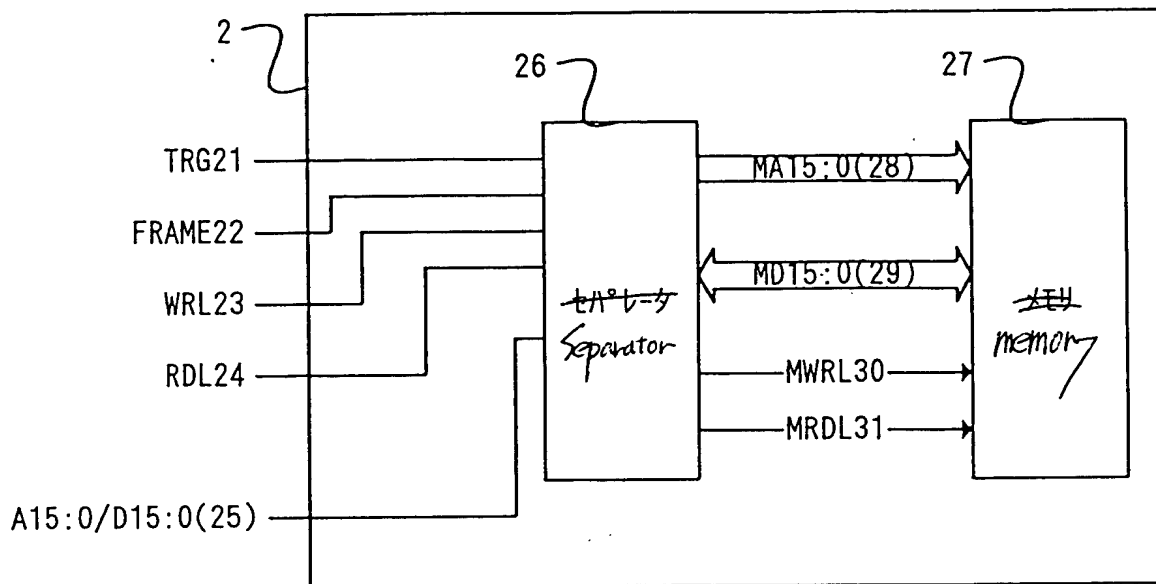
Fig. 1



Secondary board.

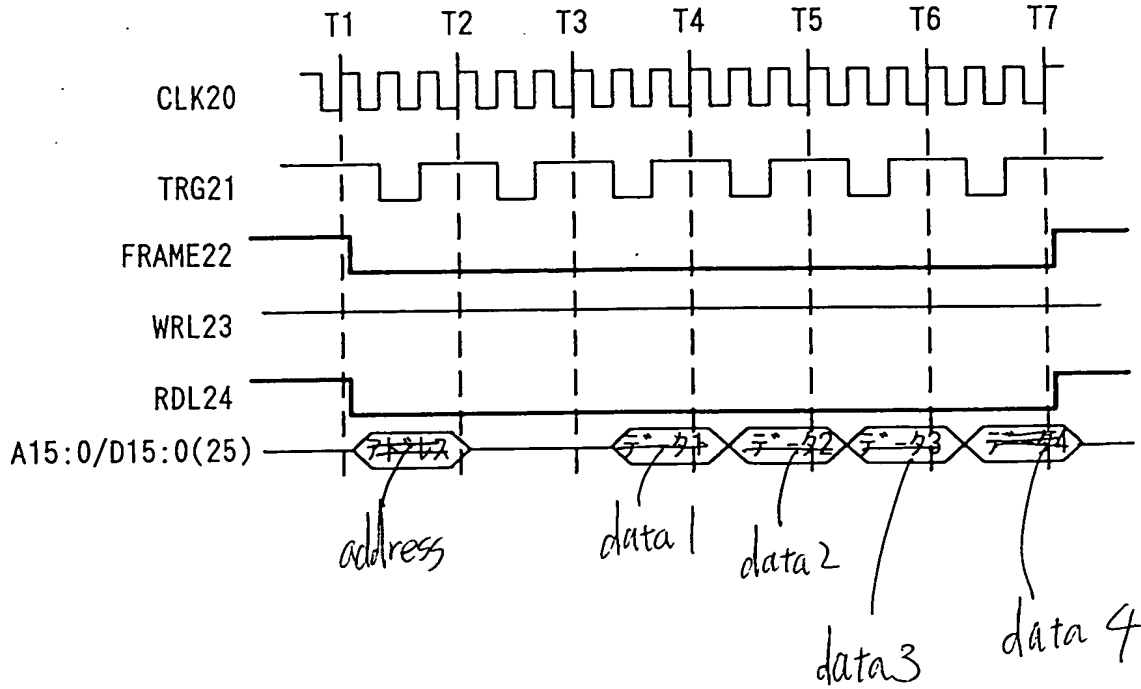
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Fig. 2



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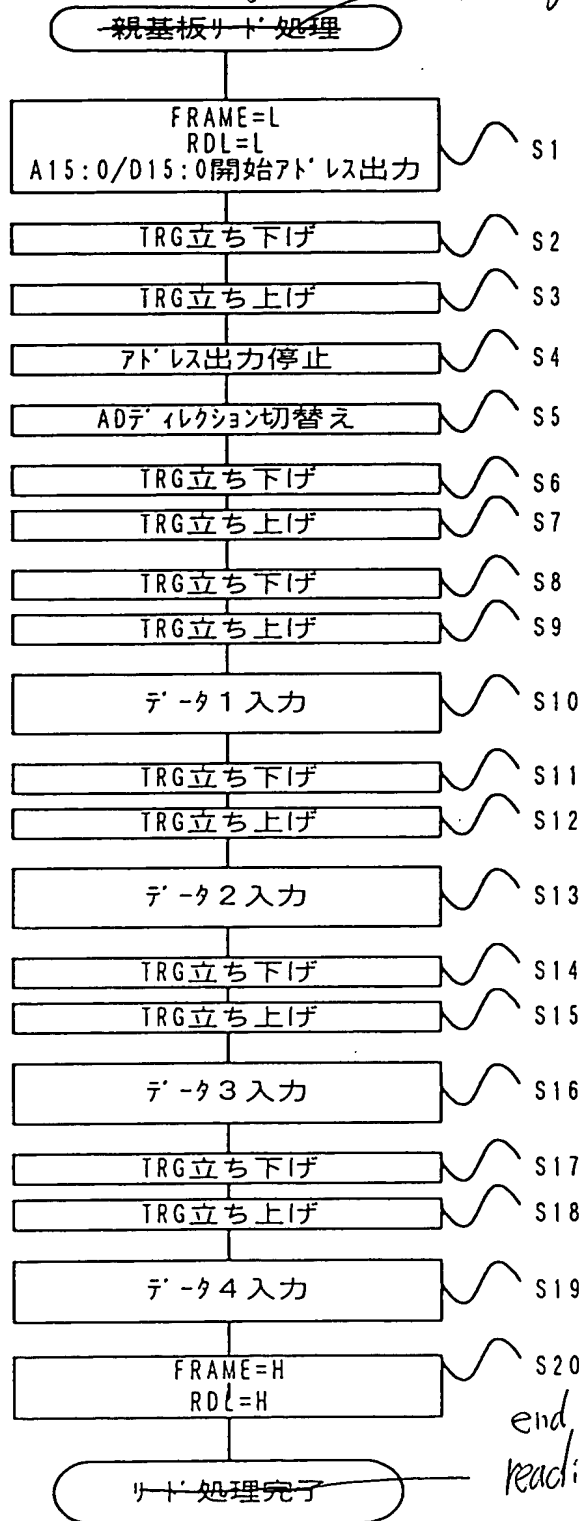
Fig. 3



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Fig. 4

reading process of
Primary board



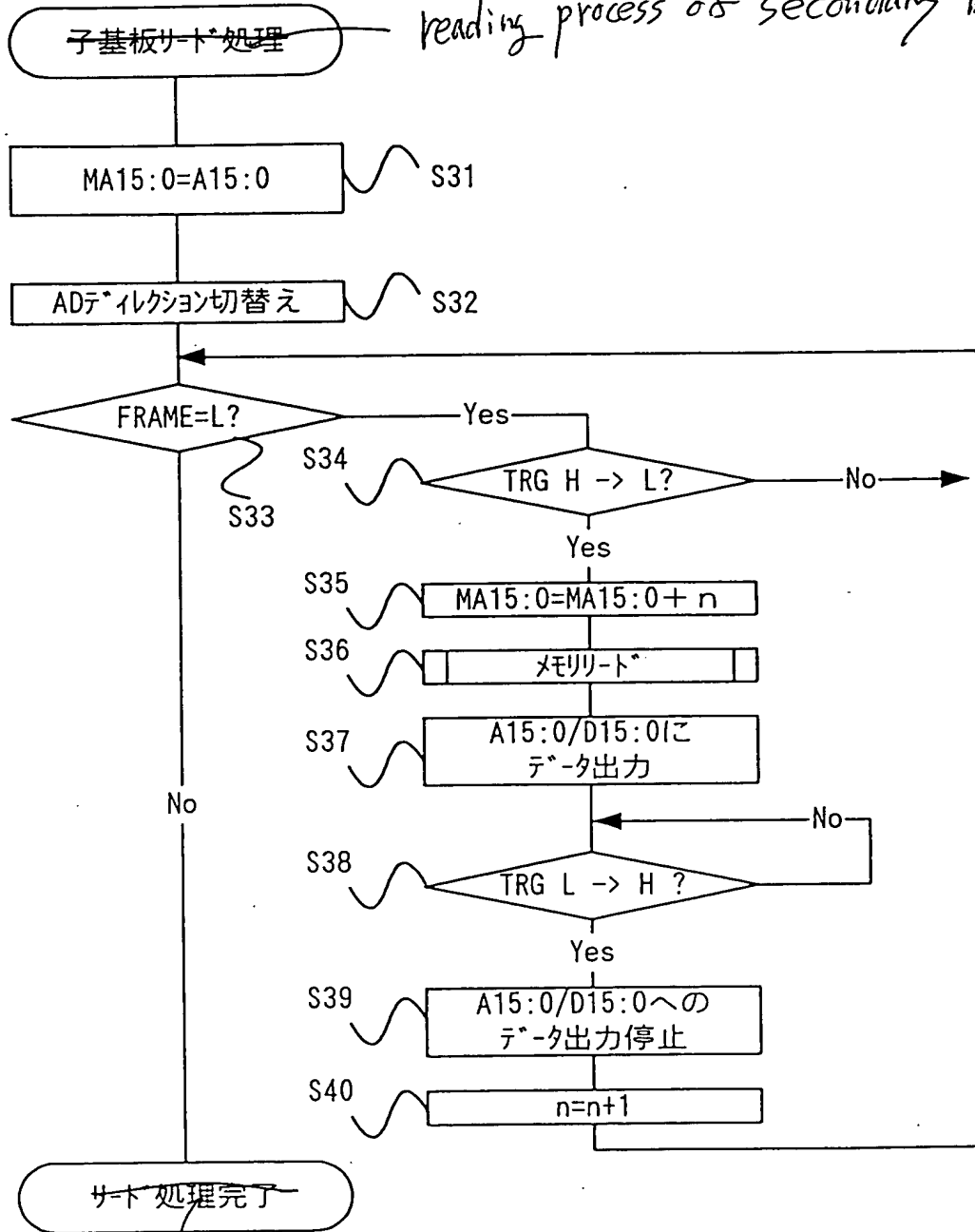
- (S1) FRAME=L, RDL=L, A15:0/D15:0 start address output
- (S2, S6, S8, S11, S14, S17) cause TRG to fall down
- (S3, S7, S9, S12, S15, S18) raise TRG
- (S4) stop address output
- (S5) switch AD direction
- (S10) input data 1
- (S13) input data 2
- (S16) input data 3
- (S19) input data 4

end of
reading process

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Fig. 5

reading process of secondary board

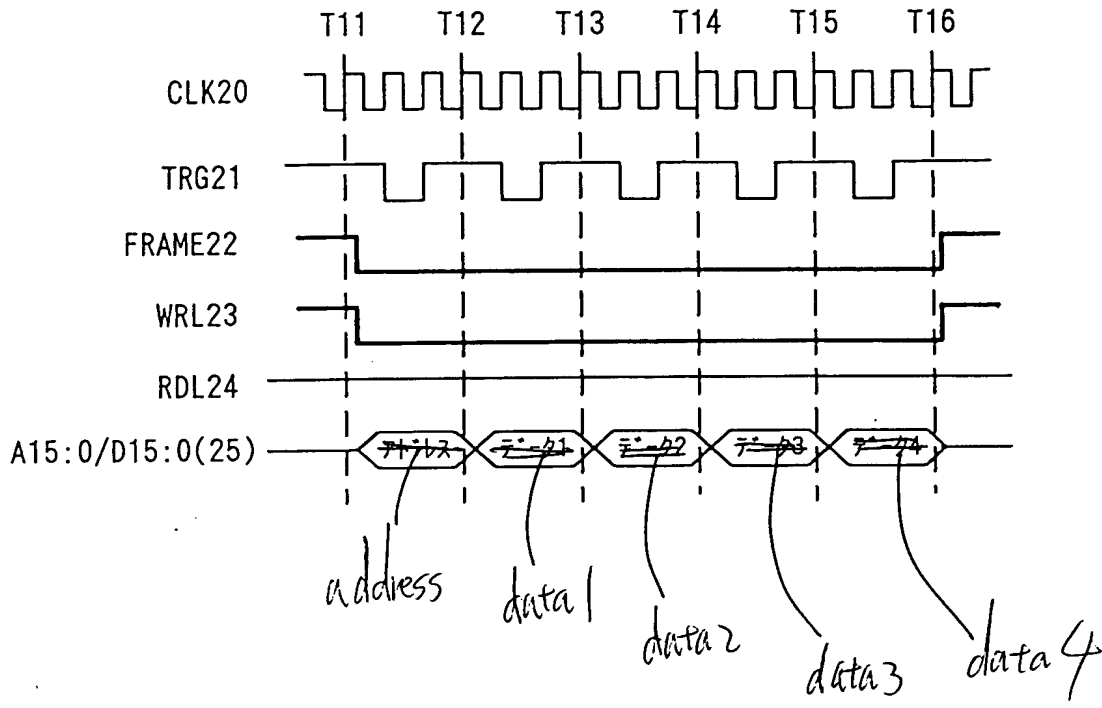


end of
reading process.

FIG. 5:
(S32) switch AD direction
(S36) memory read
(S37) data output to A15:0/D15:0
(S39) stop the data output to A15:0/D15:0

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Fig. 6



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Fig. 7

writing process of primary board.

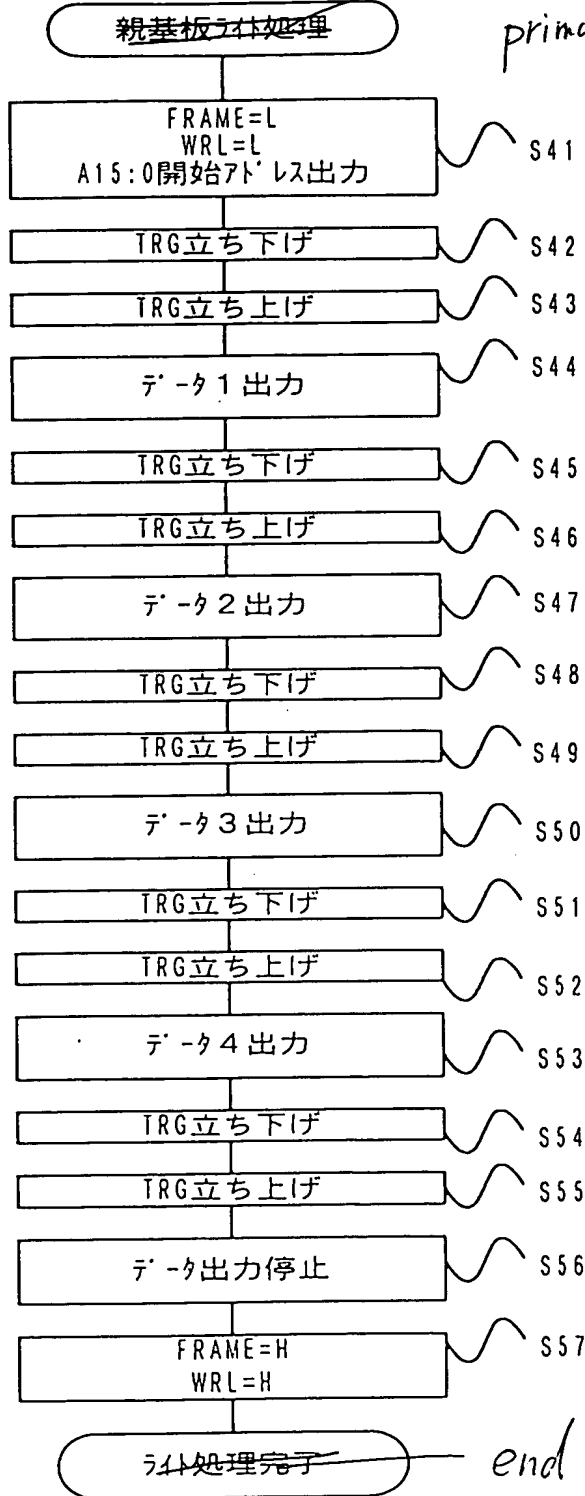
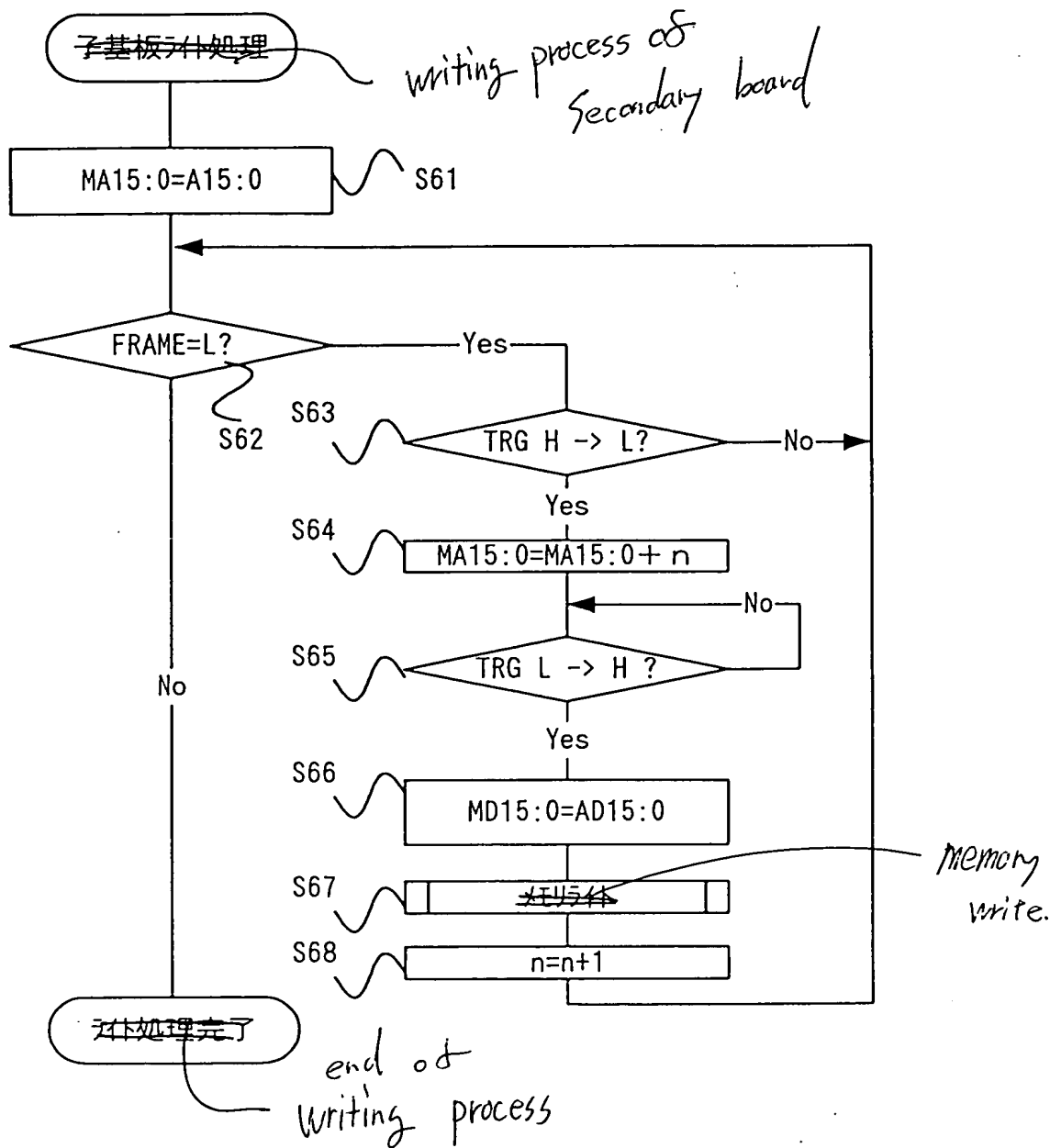


FIG.7:
 (S41) FRAME=L, WRL=L, A15:0 start address output
 (S42, S45, S48, S51, S54, S57) cause TRG to fall down
 (S43, S46, S49, S52, S55, S58) raise TRG
 (S44) output data 1
 (S47) output data 2
 (S50) output data 3
 (S53) output data 4
 (S56) stop data output

end of writing process

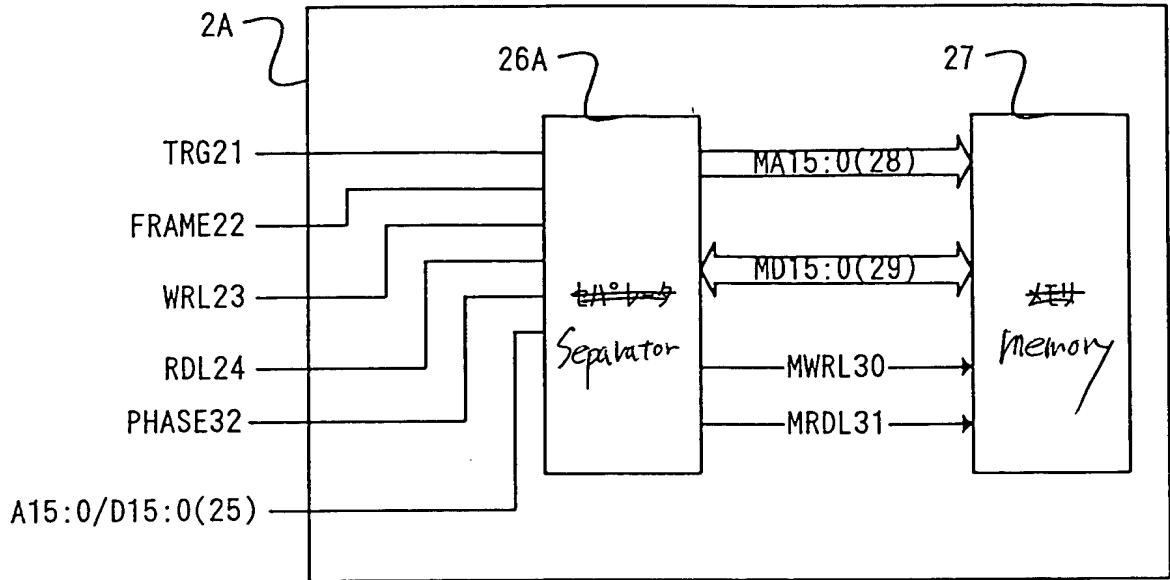
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Fig. 8



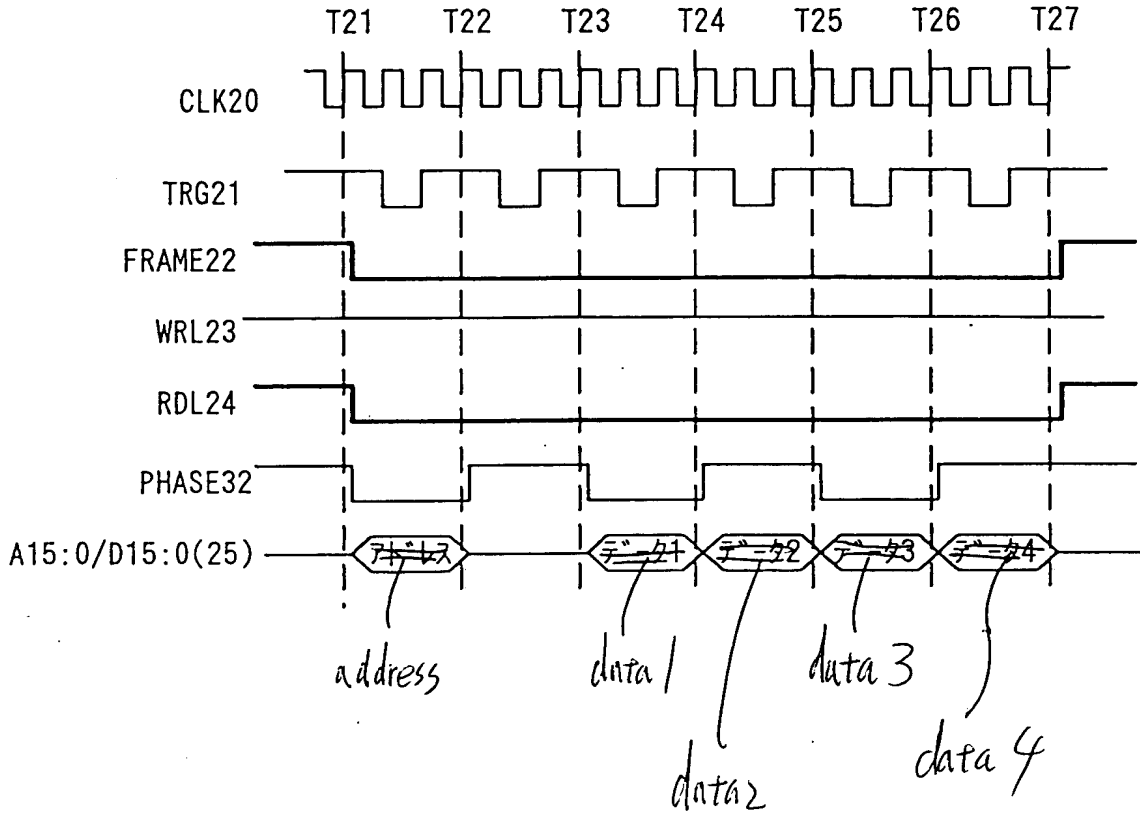
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Fig. 9



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Fig. 10



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Fig. 11.

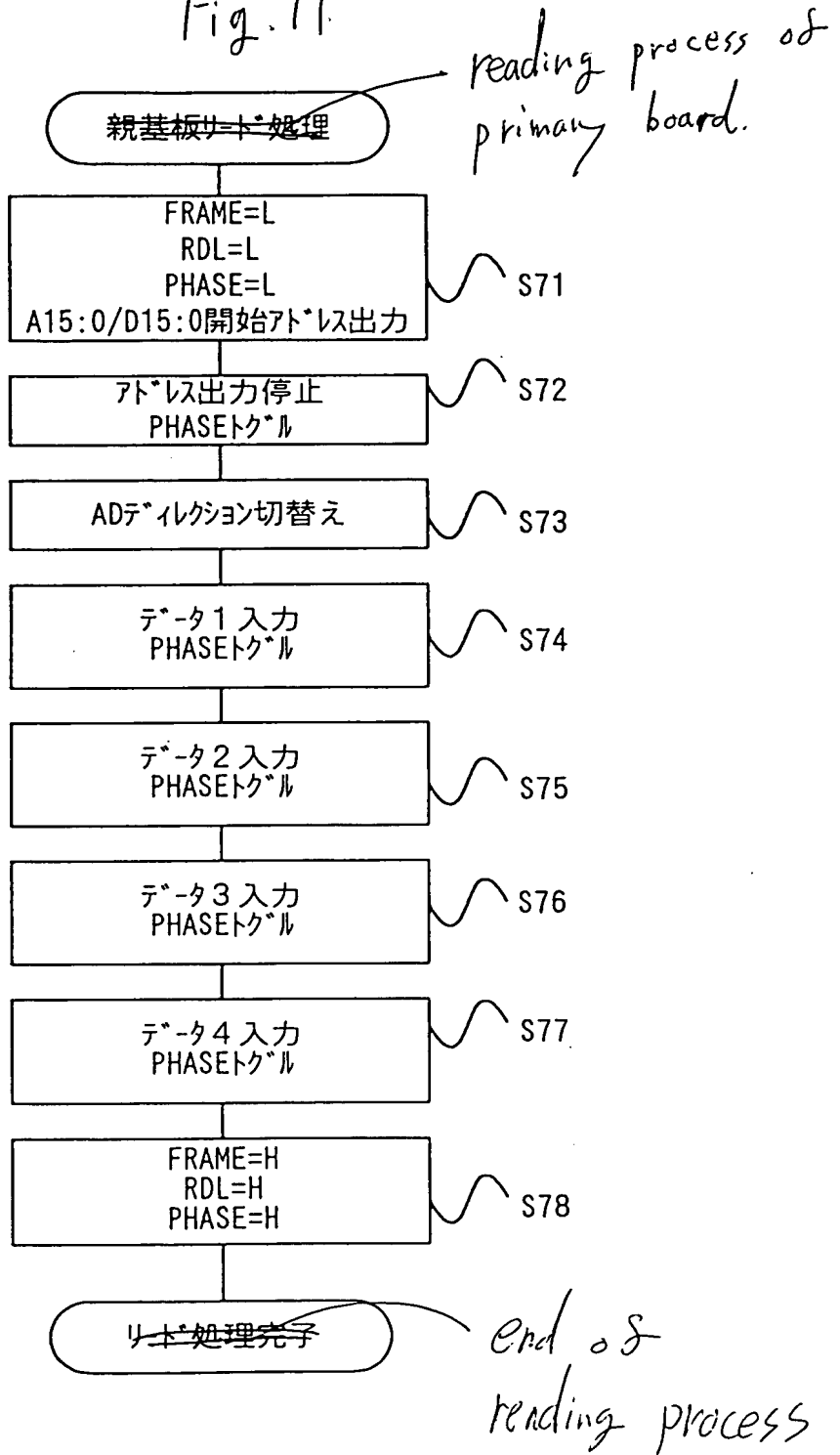


FIG. 11:
(S71) FRAME=L, RDL=L, PHASE=L, A15:0/D15:0 start address output
(S72) stop address output, PHASE toggle
(S73) switch AD direction
(S74) input data 1, PHASE toggle
(S75) input data 2, PHASE toggle
(S76) input data 3, PHASE toggle
(S77) input data 4, PHASE toggle

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Fig. 12

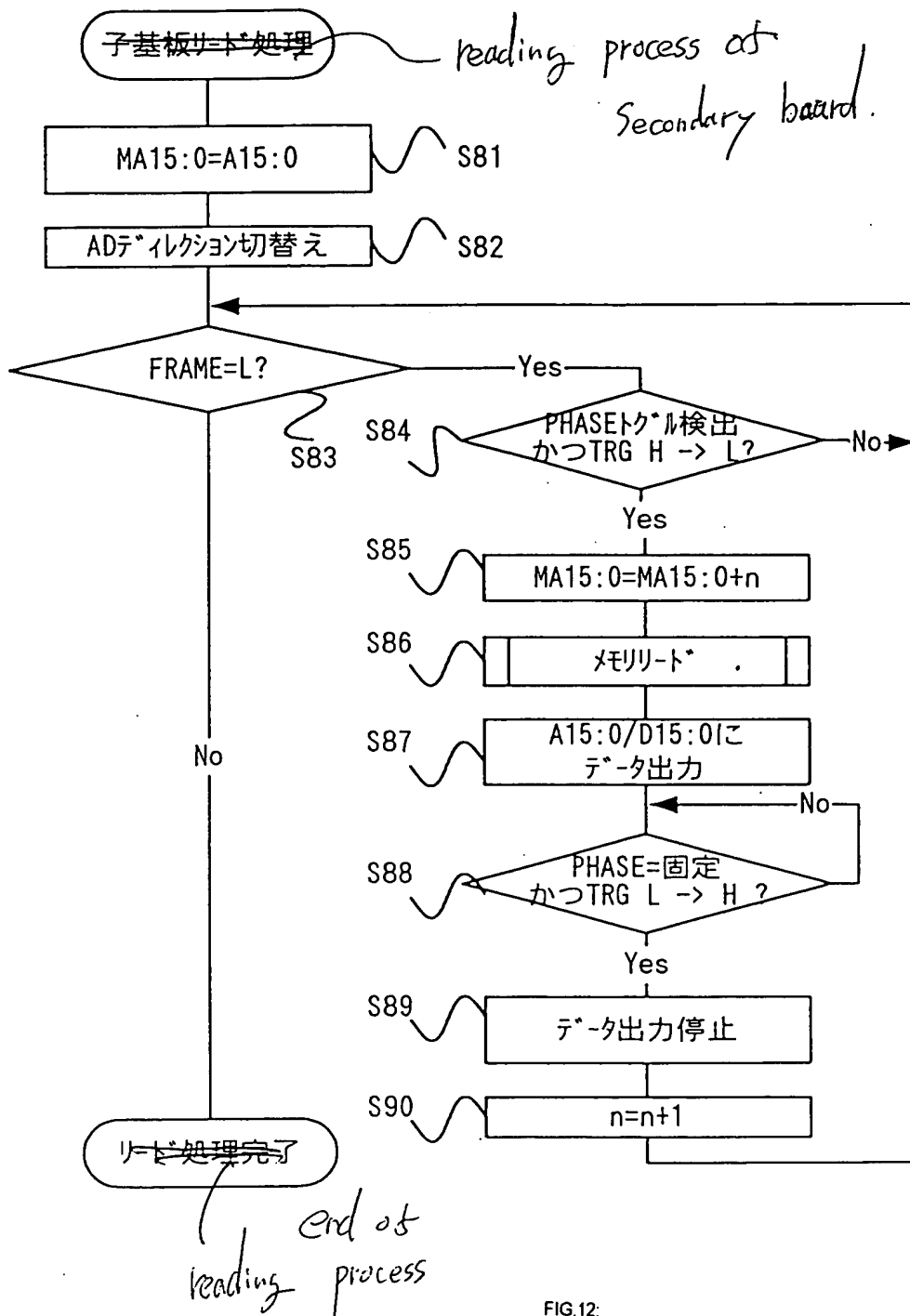
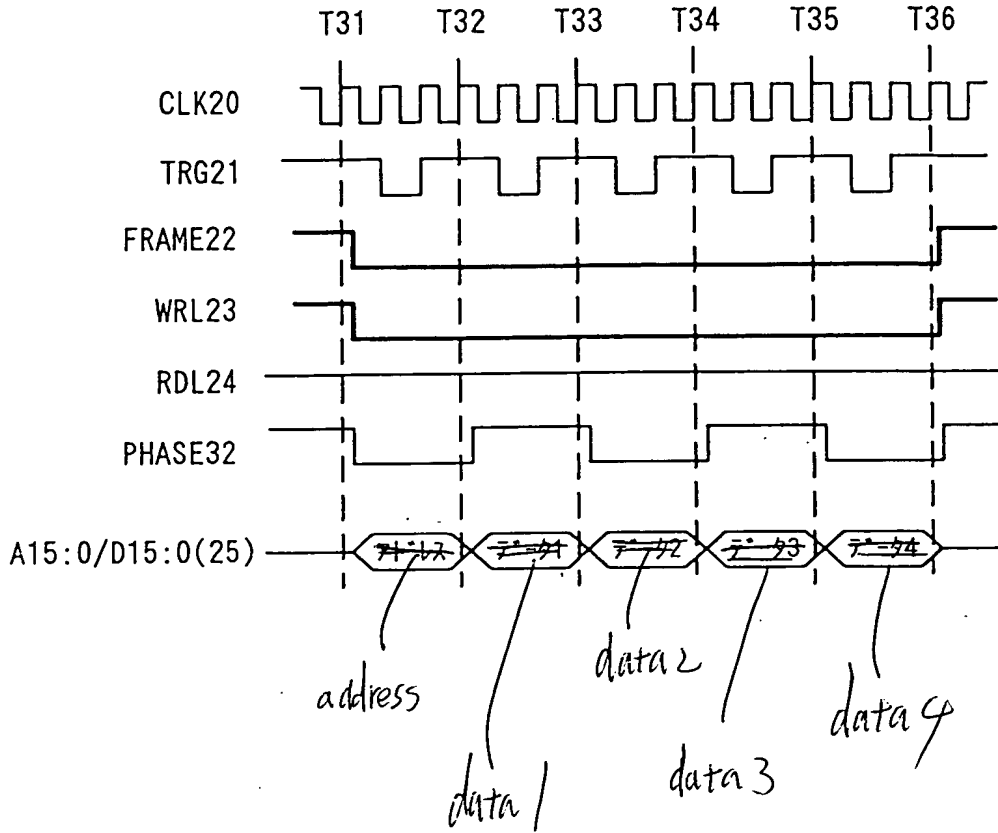


FIG. 12:
 (S82) switch AD direction
 (S84) PHASE toggle detected and TRG H→L ?
 (S86) memory read
 (S87) output the data to A15:0/D15:0
 (S88) PHASE=fixed and TRG L→H ?
 (S89) stop data output

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Fig. 13



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Fig. 14

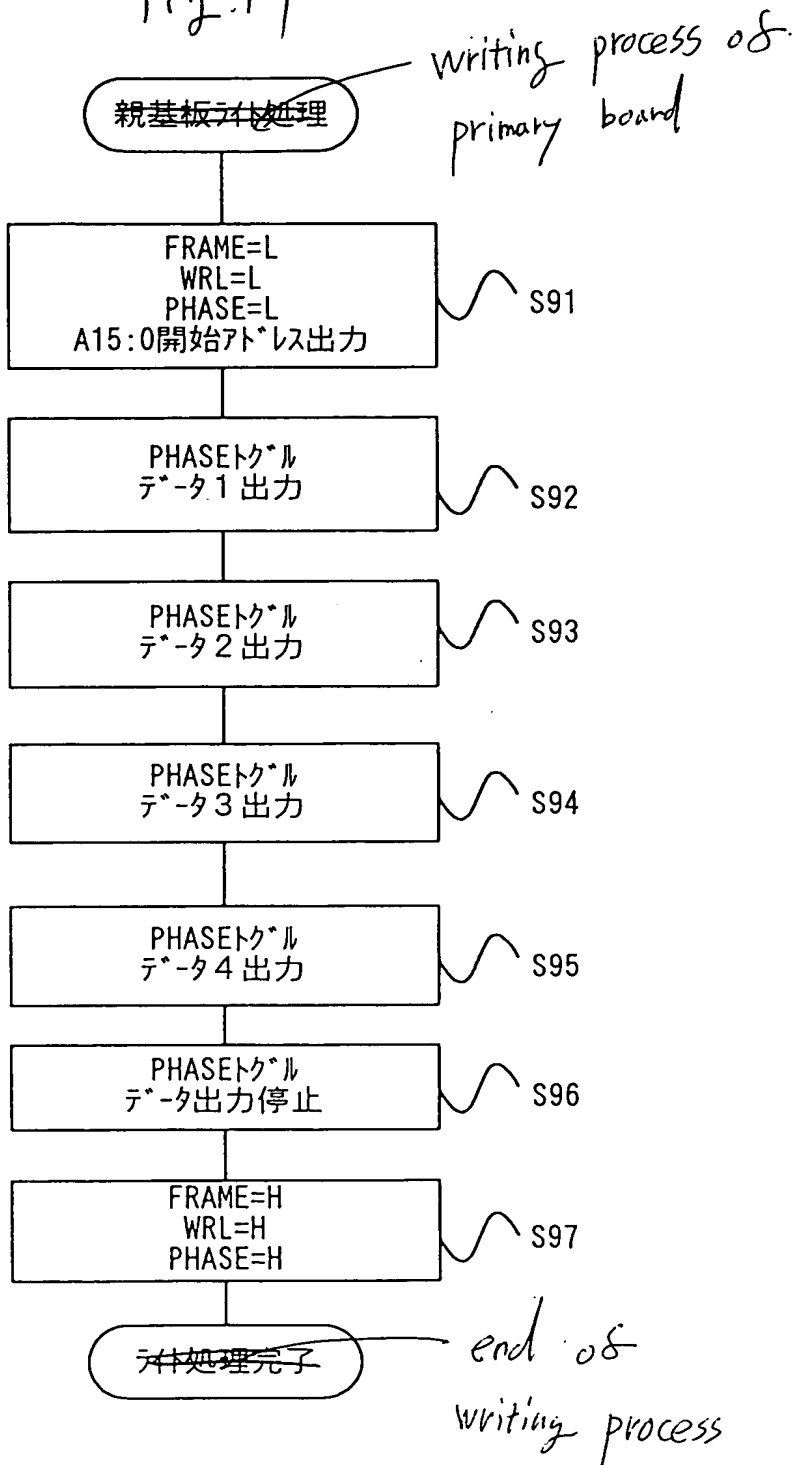


FIG. 14:

(S91) FRAME=L, WRL=L, PHASE=L, A15:0 start address output.

(S92) PHASE toggle, output data 1

(S93) PHASE toggle, output data 2

(S94) PHASE toggle, output data 3

(S95) PHASE toggle, output data 4

(S96) PHASE toggle, stop data output

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Fig. 15

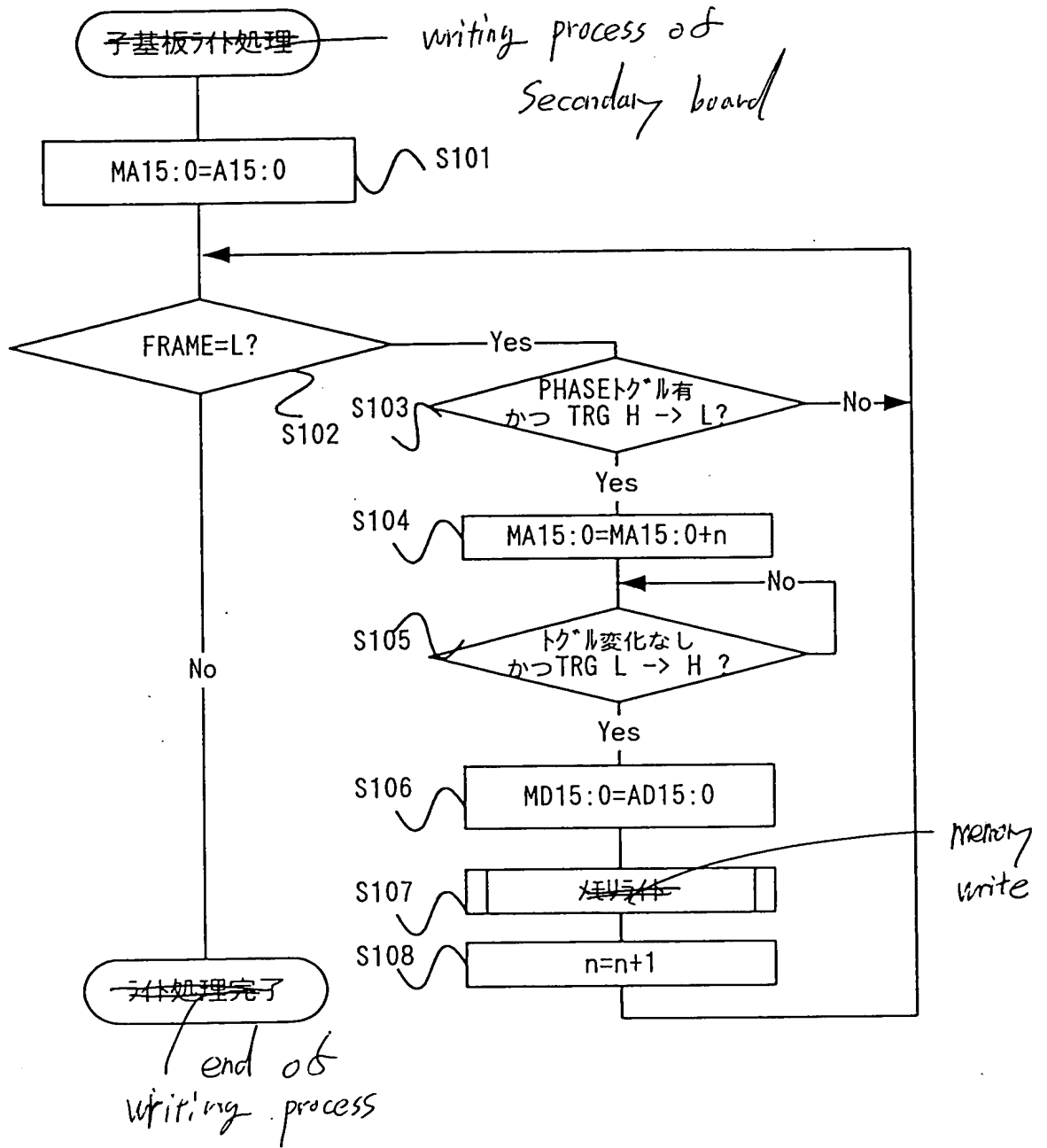
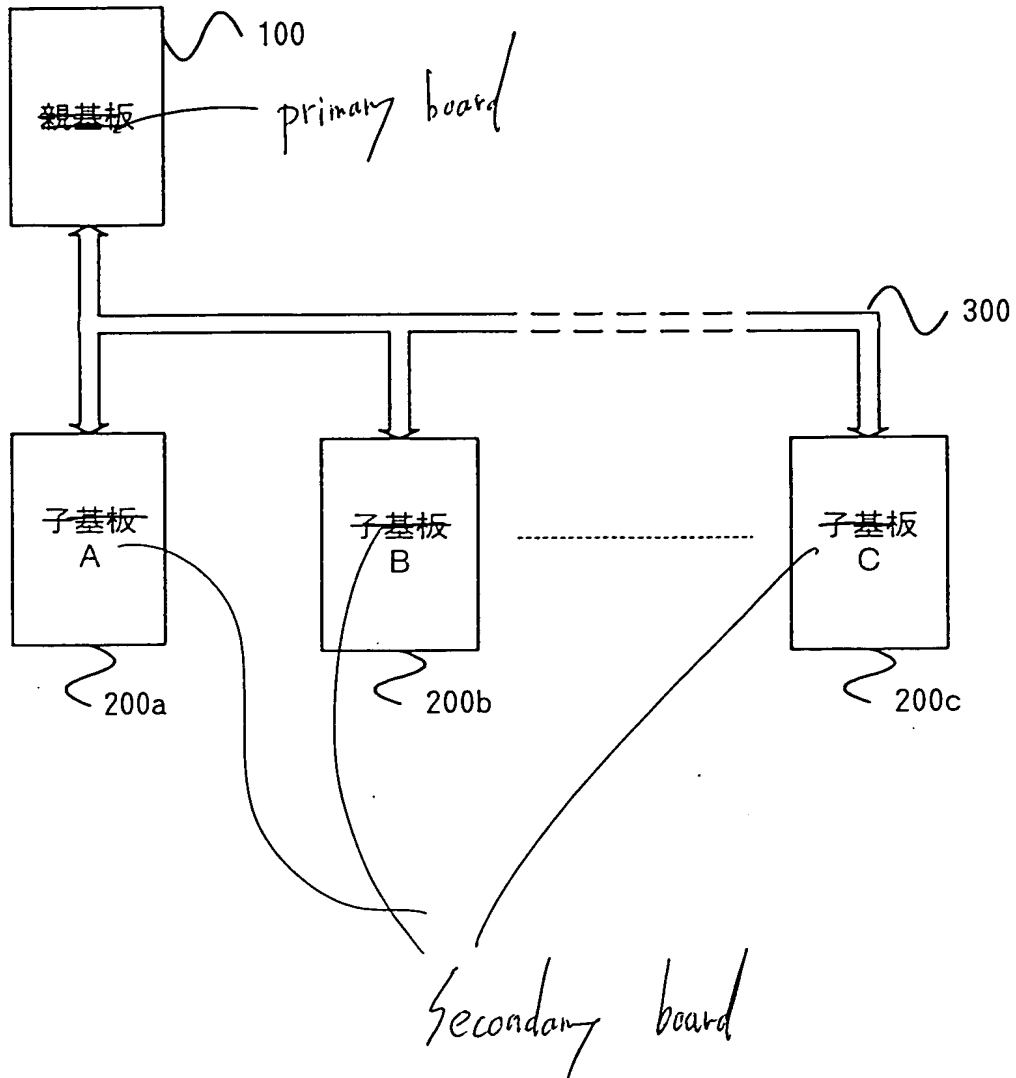


FIG. 15:
(S103) PHASE toggle and TRG H→L ?
(S105) no change in toggle and TRG L→H ?

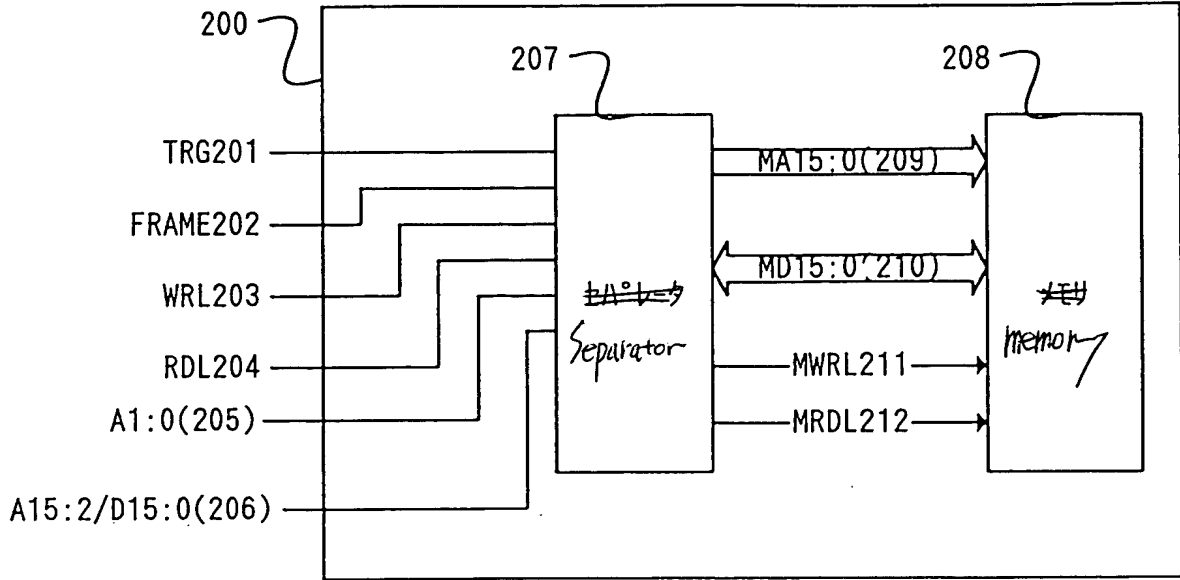
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Fig. 16



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Fig. 17



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Fig. 18

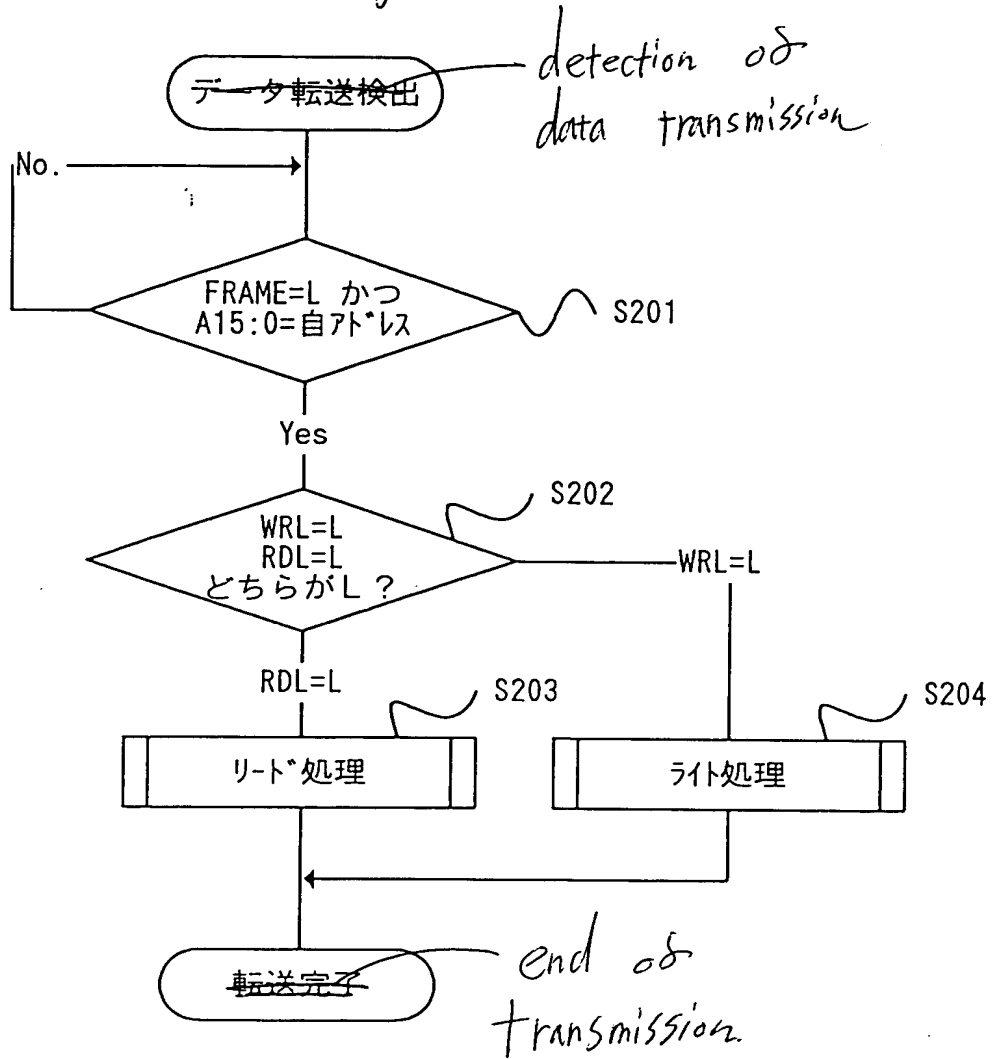
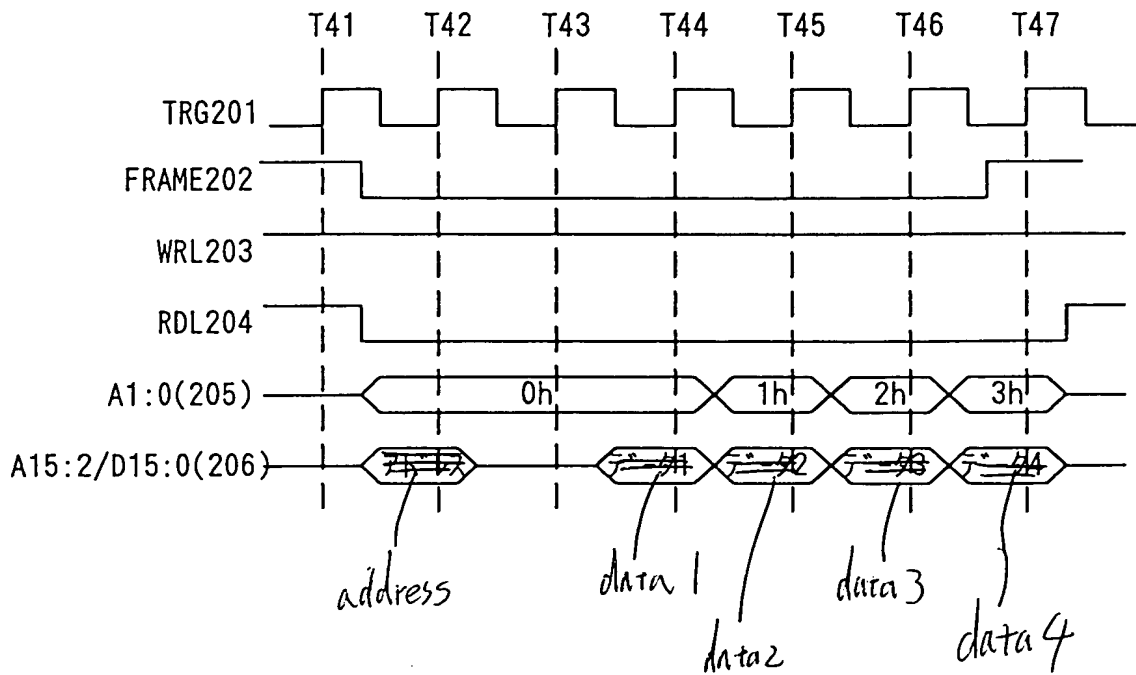


FIG. 18:
(S201) FRAME=L and A15:0=own address
(S202) which is L, WRL=L or RDL=L ?
(S203) reading process
(S204) writing process

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Fig. 19



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Fig. 20

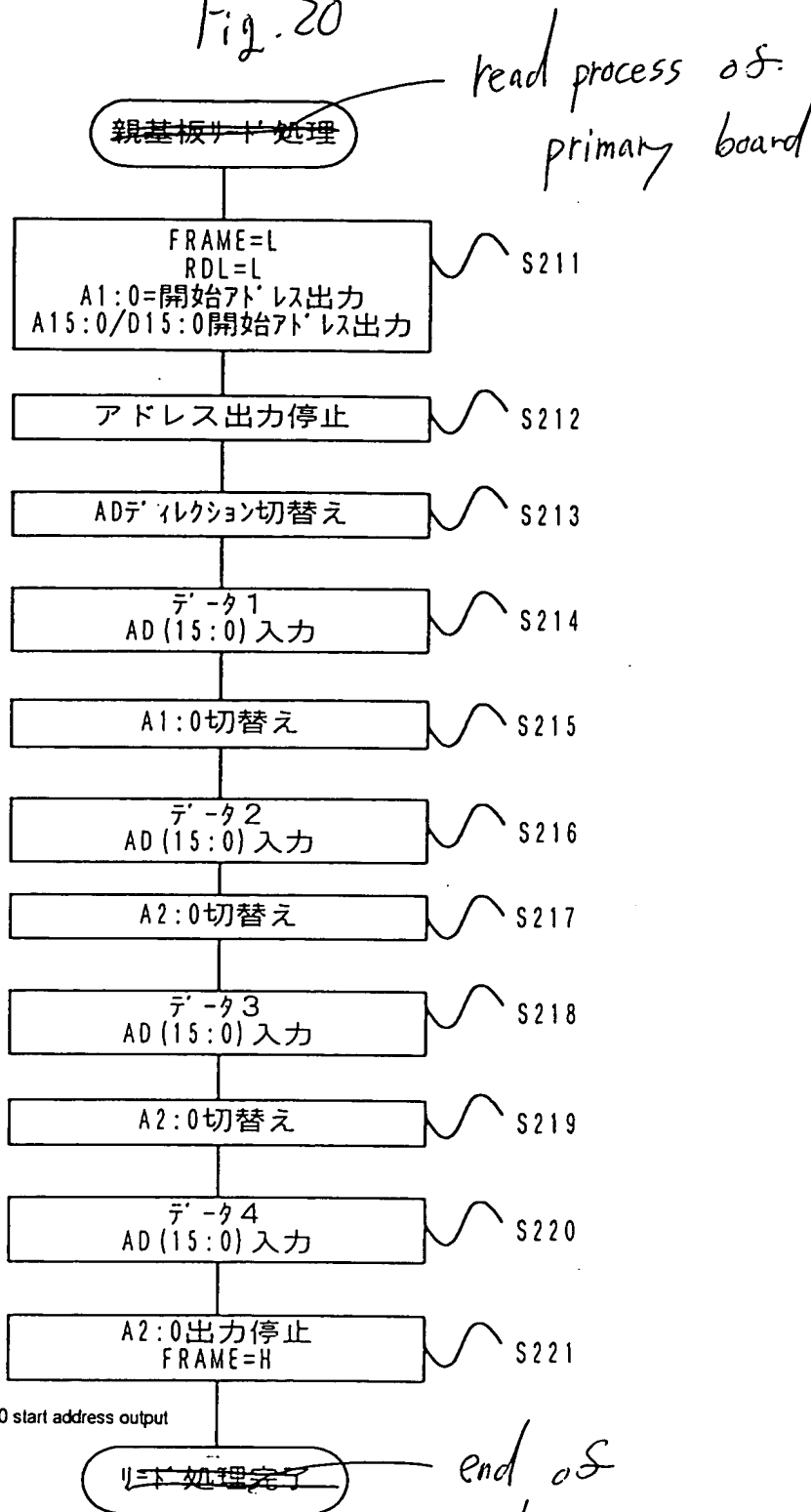


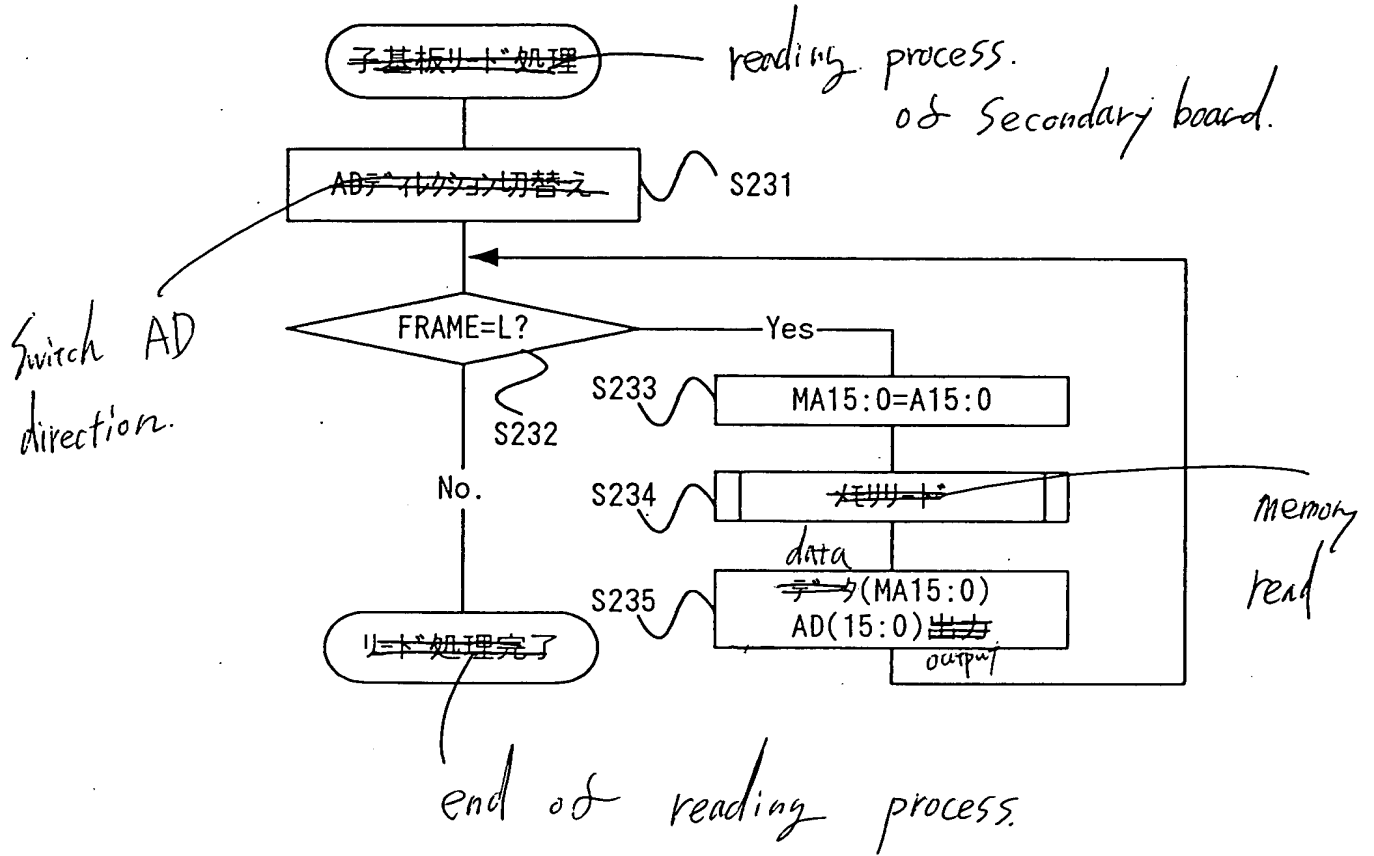
FIG. 20:
(S211) FRAME=L, RDL=L, A1:0=start address output, A15:0/D15:0 start address output
(S212) stop address output
(S213) switch AD direction
(S214) data 1, AD(15:0) input
(S215) A1:0 switch
(S216) data 2, AD(15:0) input
(S217) A2:0 switch
(S218) data 3, AD(15:0) input
(S219) A2:0 switch
(S220) data 4, AD(15:0) input
(S221) A2:0 output stop, FRAME=H

read process of
primary board

end of
reading process

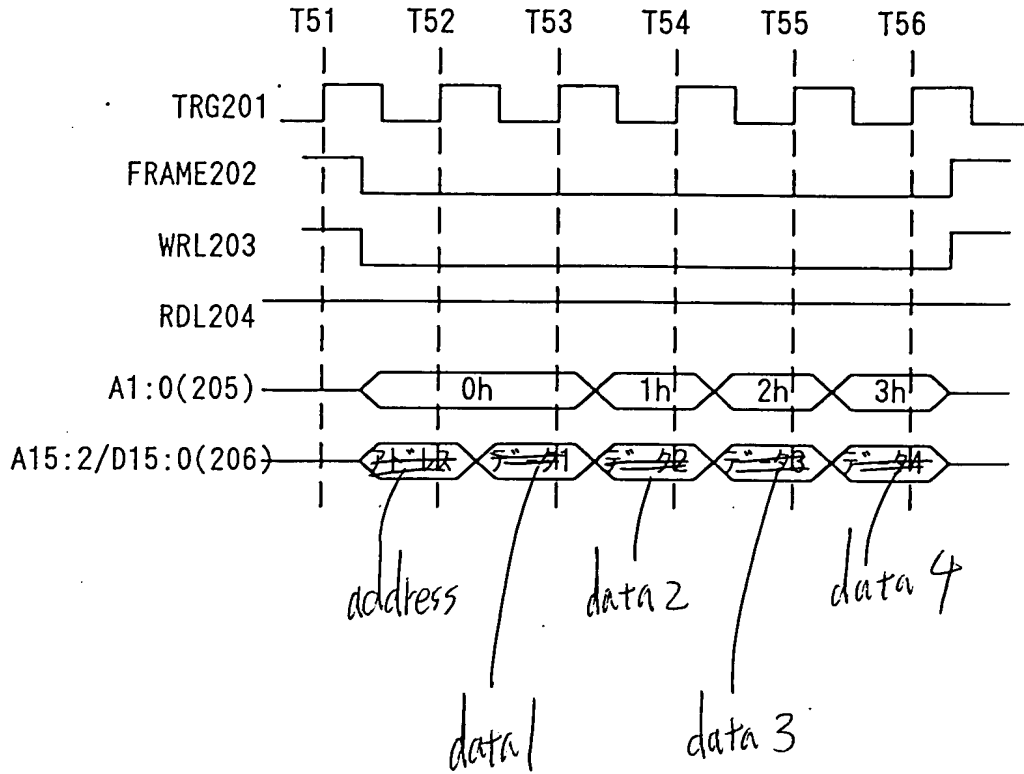
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Fig. 21



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Fig. 22

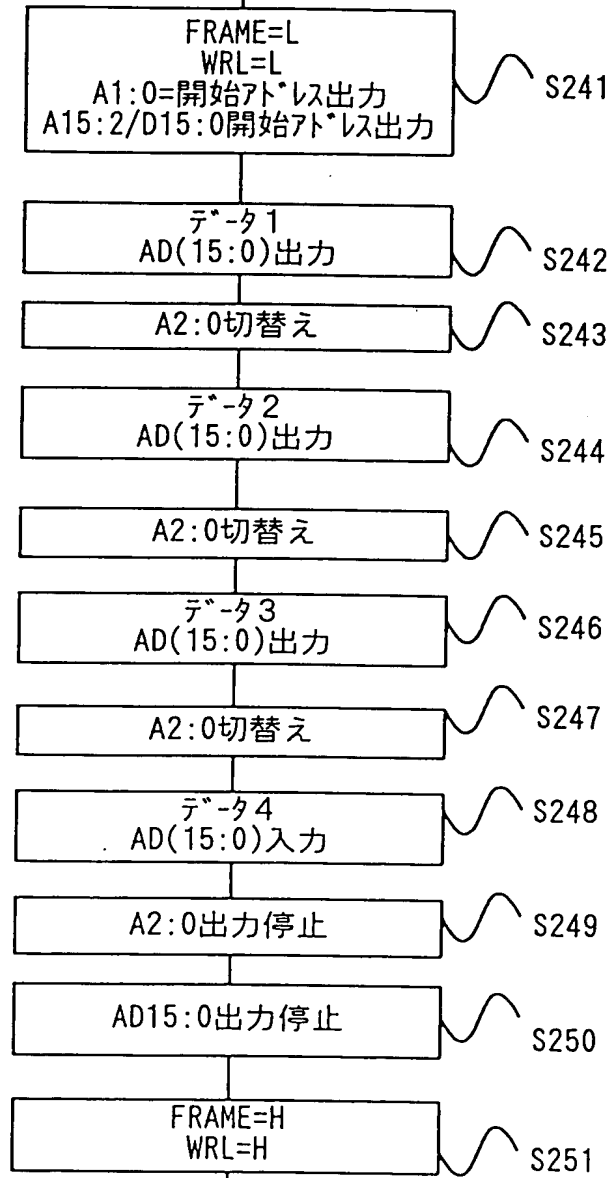


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Fig. 23

~~親基板元件処理~~

writing process.
of primary board



~~元件処理完了~~

end of
writing process

- (S241) FRAME=L, WRL=L, A1:0=start address output, A15:2/D15:0 start address output
- (S242) data 1, AD(15:0) output
- (S243) A2:0 switch
- (S244) data 2, AD(15:0) output
- (S245) A2:0 switch
- (S246) data 3, AD(15:0) output
- (S247) A2:0 switch
- (S248) data 4, AD(15:0) output
- (S249) A2:0 output stop
- (S250) AD15:0 output stop

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Fig. 24

